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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,746	01/27/2004	Tie Wang	27-013	2840

22898 7590 03/15/2006

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,746	WANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the Amendment filed 12/2/05

Claim Rejections - 35 USC § 112

1. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims recite the limitation of "encapsulating all of the volume around the semiconductor devices." It is unclear as to what the metes and bounds of this limitation might encompass, as "all of the volume around the semiconductor devices" defines an infinite space. Furthermore, the specification and drawings of the application indicate that only the areas around the devices unoccupied by the substrate, the underfill, the heat spreader, and the thermal interface material are filled by the encapsulant. It is unclear whether the Applicant is trying to claim that all of the volume immediately surrounding the semiconductor device (except that filled by other claimed components) is filled with the encapsulant; whether the volume around the semiconductor device and between the heat spreader and substrate is filled by only the encapsulant, or whether the assembly itself consists only of the claimed substrate, underfill, heat spreader, semiconductor device, and thermal interface material, with the encapsulant filling all other space in the die package. For the purpose of examination, the examiner is interpreting the "all of the volume" limitation according to the first situation listed supra (i.e., the volume immediately surrounding the semiconductor device (except that filled by the other claimed components) is filled with encapsulant.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,933,176 to Kirloskar et al.

Regarding claims 1, 6, 11, 15, 16, and 20, Kirloskar discloses a method for fabricating a semiconductor package, comprising: providing a substrate (122) in a continuous strip format (figures 3a-3b; column 4, lines 15-17); attaching semiconductor devices (124) in a continuous strip format to the substrate (figure 3b; column 4, lines 18-26); applying an underfill between the semiconductor devices and the substrate (column 4, lines 26-30); applying a thermal interface material (136) to the upper faces of the semiconductor devices opposite the substrate (figures 3F, 7F; column 4, lines 38-42; column 6, lines 10-24); attaching a flat panel heat spreader assembly (see figure 5F and 7E; 132 and 136 make up the heat spreader assembly) to each semiconductor device by means of the thermal interface material (figures 3I, 5I, 7H); curing the thermal interface material (column 6, lines 10-24); encapsulating the semiconductor devices and portions of the flat panel heat spreader (column 4, line 60 – column 5, line 3) with open encapsulation, leaving the surface of the heat spreader opposite the substrate externally exposed (figures 3I, 5I); attaching ball grid arrays (130) to the substrate opposite the semiconductor devices (see figures 3I, 3J; column 5, lines 4-15); and singulating individual semiconductor packages from the strip format (column 5, lines 15-19; figure 3I-3J). Note that Kirloskar discloses that all of the volume immediately surrounding the semiconductor device except that occupied by the substrate, the underfill, the heat spreader assembly, and the thermal interface material is occupied by the encapsulant (see figures 3I, 5I).

Regarding claims 2, 7, 12, and 17, Kirloskar discloses that the flat panel heat spreader may be applied in a pre-cut flat panel configuration (column 6, lines 1-15; figure 7G).

Regarding claims 3, 4, 8, 9, 13, 14, 18, and 19, Kirloskar discloses that the heat spreader is a continuous flat panel heat spreader attached over substantially the entire strip format (figures 3D, 3I; column 4, lines 30-37), and that the heat spreader is cut into individual panels following the attachment of the heat spreader (figures 3I-3J; heat spreader is cut into individual panels during the singulation step, which occurs after attaching the heat spreader).

Regarding claims 5 and 10, Kirloskar discloses that the heat spreader is attached by the encapsulant, and hence, must necessarily be physically attached after the encapsulant is dispensed (see Kirloskar, column 4, line 60 – column 5, line 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-9, and 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,734,552 to Combs et al. in view of U.S. Patent No. 5,450,283 to Lin et al.

Regarding claims 1, 6, 11, 15, 16, and 20, Combs discloses a method for fabricating a semiconductor package, comprising: providing a substrate (100) in a strip format (column 3, lines 50-55), attaching semiconductor devices (130) in a strip format to the substrate (column 4,

lines 20-25); applying a thermal interface material (119, 120) to the upper faces of the semiconductor devices (column 5, lines 35-45; column 6, lines 1-15); attaching a flat panel heat spreader (110, 112) to each semiconductor device (column 5, lines 1-20); encapsulating all of the volume around the semiconductor devices not occupied by the other claimed components (see figures 1, 3) with open encapsulation, leaving the surface of the heat spreader opposite the substrate externally exposed (figure 1; column 5, lines 20-35; column 6, lines 15-25); attaching a ball grid array (106) and singulating individual packages from the strip format (column 6, lines 28-37). Combs indicates that the semiconductor device may be a flip chip (see figure 3), but fails to specifically disclose applying an underfill between the devices and the substrate.

Lin discloses that it is standard in the art to apply an underfill between a flip chip device and a substrate in order to reduce the thermal mismatch between the chip and substrate, thus reducing the risk of breakage of the solder joints. Lin further indicates that underfills are advantageous in providing additional protection for the die from contaminants (see column 3, line 60 – column 4, line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method and device of Combs, such that an underfill is applied between the device and the substrate, as suggested by Lin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide an underfill, in order to reduce the thermal stress on the solder joints, minimize the thermal mismatch between the substrate and die, and provide environmental protection for the active surface of the die (see Lin, column 3, line 40 – column 4, line 15).

Regarding claims 2, 7, 12, and 17, Combs discloses that the heat spreaders can be pre-cut (column 5, lines 1-6).

Regarding claims 3, 4, 8, 9, 13, 14, 18, and 19, Combs discloses that the heat spreaders can be provided in a continuous flat panel (figures 9a, 9b; column 5, lines 1-20) and cut into individual heat spreader panels (upon singulation).

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2001/0019181 to Lee et al. in view of U.S. Patent No. 6,534,858 to Akram et al.

Regarding claims 1, 6, 11, 15, 16, and 20, Lee discloses a method for fabricating a semiconductor package, comprising: providing a substrate in continuous strip format (figure 5c), attaching devices (22) in a continuous strip format to the substrate (figures 5c-5e), applying a thermal interface material to the upper faces of the devices (see figures 2, 5d; paragraph 0025; noting that the thermal interface material is directly applied to the semiconductor device in the figure 2 embodiment, and in the figure 5d embodiment, the thin portion of the molding compound as well as the glue layer can be considered a thermal interface, as it enables heat transfer from the die to the heat spreader), encapsulating all of the volume immediately surrounding the chip, other than that occupied by the other claimed chip components (see figures 3-5f) with open encapsulation, leaving the surface of the heat spreader opposite the substrate externally exposed (figures 2, 3, 4, 5f), attaching ball grid arrays (figure 5e); and singulating the individual packages (figure 5f).

Lee fails to disclose applying an underfill between the devices and the substrate, but rather only discloses an epoxy adhesive.

Akram discloses that flip chip bonding (figure 4), TAB bonding, and wirebonding (figure 6) methods for chip-on-board attachment to a substrate are well-known in the art, are analogous, and generally use substantially similar package architectures, except for the placement of the electronic connections to the substrate (compare figures 4 and 6, for example; also see column 1, line 28 – end of column 3). Akram further teaches that it is standard to apply an underfill material between a chip and a substrate for flip chip bonding (see column 2, lines 15-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lee, such that the wirebonded chip is replaced by a flip chip with an underfill, as suggested by Akram. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use flip chips in the structure of Lee, because Akram shows that substantially the same package architecture, including the same approaches to thermal management are applied for both flip chip and wirebonded chip-on-board devices (see Akram, columns 1-3). It would thus be a matter of routine skill in the art to apply the method and structure taught by Lee to devices attached by any of the chip-on-board methods taught by Akram, in order to achieve the improved heat dissipation of the Lee-type package (see Lee, paragraphs 0009, 0010, 0030). Furthermore, a person skilled in the art would generally find a flip chip and underfill arrangement preferable over a wirebonding arrangement, since the wirebonding process is generally slower, more expensive, and less reliable than a flip chip process, and since the underfill material is selected to provide greater thermal matching between the substrate and the chip, as is well-known in the art.

Regarding claims 2-4, 7-9, 12-14, and 17-19, Lee discloses that the heat spreader is provided either pre-cut (see figure 5d – individual heat spreader elements are applied over each

chip), or provided in a continuous panel (figure 5d; heat spreader is applied as a continuous sheet).

Regarding claims 5 and 10, Lee discloses dispensing the encapsulant prior to attaching the heat spreader (see figures 5c-5e; figures 0028-0029).

Response to Arguments

6. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new grounds of rejection.

The examiner notes that the Applicant has added the claim language of encapsulating "all of the volume around the semiconductor devices" in order to overcome the rejections based on Kirloskar et al. The Applicant, however, only discloses encapsulating the area between the heat spreader and the substrate not occupied by the other claimed elements, such as the solder balls for the flip chip, the underfill, and the thermal interface material. Since the collapsible spacers in Kirloskar could either be considered to be part of the heat spreader (figure 5F shows the spacers 136 and spreader 132 as one integral body) or part of the thermal interface material (spacers are formed of a thermally conductive material, and thus conduct heat from the substrate to the heat spreader), it appears to the Examiner that Kirloskar reads on the claim language taken in light of the Applicant's specification and disclosure (as explained in the 35 U.S.C. 112 rejections, supra).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
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jmd

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